WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a plurality of gate lines carrying scanning signals, formed on the insulating substrate, and proceeding in a transverse direction;

a plurality of data lines carrying image signals, proceeding in a longitudinal direction to intersect the gate lines, and insulated from the gate lines;

a plurality of pixel electrodes formed in respective pixels defined by intersections of the gate lines and the data lines and receiving the image signals; and

a plurality of thin film transistors formed in the pixels and having gate electrodes connected to the gate lines, source electrodes connected to the data lines, and drain electrodes connected to the pixel electrodes,

wherein a ratio of horizontal to vertical of each pixel is substantially equal to 2:3.

2. The thin film transistor array panel of claim 1, wherein the pixel electrodes overlap previous gate lines for transmitting the scanning signals to previous adjacent pixel rows to form storage capacitors.

3. The thin film transistor array panel of claim 1, further comprising a plurality of storage electrode lines separated from the gate lines, formed of the same layer as the gate lines, and overlapping the pixel electrodes to form storage capacitors.

4. The thin film transistor array panel of claim 1, further comprising a protective layer formed between the pixel electrodes and the gate lines and the data lines, made of acryl-based organic insulating material or chemical vapor deposited insulating material having a dielectric constant equal to or less than 4.0, and having a plurality of contact holes for electrically connecting the pixel electrodes to the drain electrodes.

5. The thin film transistor array panel of claim 1, wherein the data lines have a triple-layered structure including an amorphous silicon layer, an ohmic contact layer, and a metallic layer.

6. The thin film transistor array panel of claim 1, wherein the pixel electrodes have cutouts.

7. The thin film transistor array panel of claim 1, wherein a data pad for receiving data signals from an external device is connected to each data line.

8. A liquid crystal display comprising:

a first insulating substrate;

a plurality of gate lines carrying scanning signals, formed on the first insulating substrate, and proceeding in a transverse direction;

a plurality of data lines carrying image signals, proceeding in a longitudinal direction to intersect the gate lines, and insulated from the gate lines;

a plurality of pixel electrodes formed in respective pixels defined by intersections of the gate lines and the data lines and receiving the image signals; and

a plurality of thin film transistors formed in the pixels and having gate electrodes connected to the gate lines, source electrodes connected to the data lines, and drain electrodes connected to the pixel electrodes;

a second insulating substrate facing the first insulating substrate;

a black matrix formed on the second insulating substrate;

red, green and blue color filters formed on the black matrix and provided at the respective pixels;

a common electrode formed on the color filters; and

a liquid crystal layer sandwiched between the pixel electrode and the common electrode,

wherein red, blue and green pixels are sequentially arranged in a row direction, the red and the green pixels are alternately arranged in a column

direction, the blue pixels are repeatedly arranged in the column direction, four red and green pixels surrounding adjacent two blue pixels in neighboring two pixel rows face each other, and a ratio of horizontal to vertical of each pixel is equal to 2:3.

9. The liquid crystal display of claim 8, wherein each pixel electrode has a first cutout, the common electrode has a plurality of second cutouts, and each pixel is partitioned into a plurality of domains by the first and the second cutouts.

10. The liquid crystal display of claim 9, wherein liquid crystal molecules contained in the liquid crystal layer are aligned perpendicular to the first and the second substrates in absence of electric field between the pixel electrodes and the common electrode.

11. The liquid crystal display of claim 9, further comprising a protective layer formed between the pixel electrodes and the gate lines and the data lines and having a plurality of contact holes for electrically connecting the pixel electrodes to the drain electrodes, the drain electrodes overlapping the second cutouts at least at the contact holes.